

[Delay Lock Circuit Using Bisection Algorithm and Related Method]

Abstract of Disclosure

A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock is provided. The method has correcting processes executed to increase or decrease, by a correction interval, a delay time between corresponding periods of the first clock and the second clock. The correction interval for a subsequent correcting process is substantially half the previous correction interval of the previous correcting process.

Figures

Figure 1: A line graph showing the relationship between the number of figures and the number of pages. The x-axis represents the number of figures (0 to 10) and the y-axis represents the number of pages (0 to 10). The data points are (0, 0), (1, 1), (2, 2), (3, 3), (4, 4), (5, 5), (6, 6), (7, 7), (8, 8), (9, 9), and (10, 10). The line is a straight line with a slope of 1, indicating that the number of figures is equal to the number of pages.